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Recent progress in Van der Waals (vdW) heterojunction-based electronic and optoelectronic devices

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ABSTRACT

The rediscovery of graphene in 2004 triggered an explosive expansion of research on various van der Waals (vdW) materials. The atomic layers of these vdW materials do not have surface crystal defects and are bonded by weak vdW interactions, thus the vdW materials can be stacked onto each other to form vdW heterojunction structures without needing to consider the lattice mismatch issue. In addition, the broad library of vdW materials makes it possible to design diverse types of heterojunctions with a wide range of band alignments, bandgaps, and electron affinities. Vertical vdW heterostructures especially offer numerous possibilities for the realization of high-performance electronic and optoelectronic devices. Therefore, these vdW heterostructures have received significant attention, and extensive relevant experimental results have been reported in the past few years. In this review, we first introduce the transfer techniques to form vdW heterojunction structures. Next, we discuss recent progress in vdW heterostructure-based electronic and optoelectronic devices, including vertical field effect transistors, negative differential resistance devices, memories, photodetectors, photovoltaic devices, and light-emitting diodes. Finally, we conclude this review by discussing the current challenges facing vdW heterojunction structure-based devices and our perspective on future research directions.

1. Introduction

Since the rediscovery of graphene by Geim and Novoselov et al. in 2004 [1], various theoretical and application-based studies on graphene have been conducted. However, graphene-based devices have been plagued by high leakage current issues due to the zero bandgap property of graphene. This, in turn, triggered an explosive expansion of research on van der Waals (vdW) materials with bandgaps, such as molybdenum disulfide (MoS_2), molybdenum diselenide ($MoSe_2$), tungsten disulfide (WS_2), tungsten diselenide (WSe_2), black phosphorene (BP), and hexagonal boron nitride (*h*-BN). The atoms within each layer (in-plane) of these vdW materials are held together by covalent bonds, whereas the atomic layers (out-of-plane) without dangling bonds are bonded together by weak vdW interactions [2–5]. Owing to this unique structure based on the weak vdW interactions between neighboring layers, the vdW materials can be stacked onto each other to form vdW heterojunction structures without the concern of lattice mismatch. The library of vdW materials [Fig. 1(a)] makes it possible to design heterojunctions through unique combinations of bandgaps,

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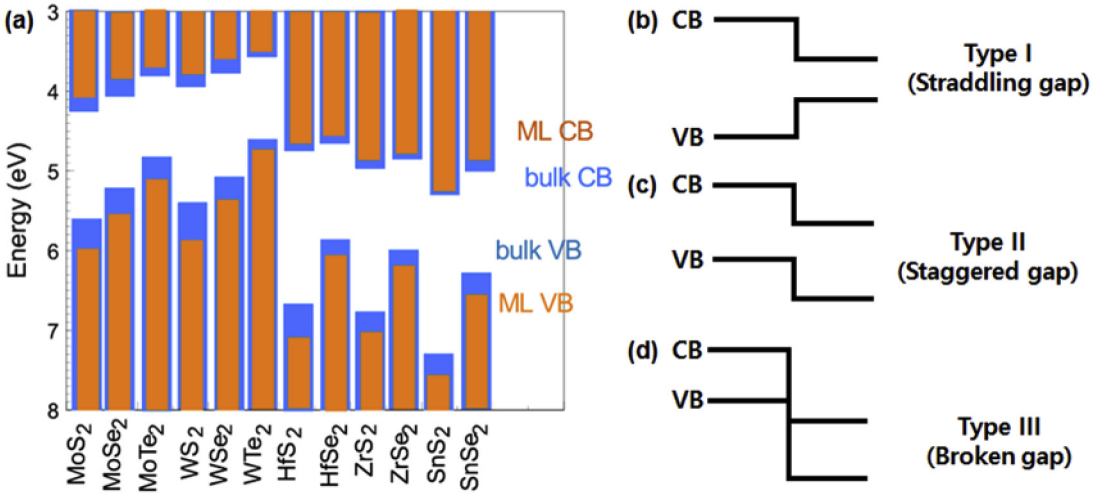

Fig. 1. (a) Calculated band alignments for vdW materials (reproduced with permission from Ref. [6] Copyright 2016, AIP Publishing). (b)–(d) Schematic energy band diagrams of the three types of semiconductor heterojunctions: (b) type-I (straddling gap), (c) type-II (staggered gap), and (d) type-III (broken gap) heterojunctions. (A colour version of this figure can be viewed online.)

electron affinities and band alignments [6,7]. These heterojunctions can be distinctly classified based on their energy band alignments: straddling gap (type-I), staggered gap (type-II), and broken gap (type-III). In type-I heterojunctions, the energy bandgap of one semiconductor lies completely within that of the other semiconductor [Fig. 1(b)]. Such heterojunction structures are useful for optoelectronic devices requiring a quantum well structure, such as light-emitting diodes (LEDs) [8–13]. In type-II heterojunctions, the bandgap of one semiconductor partially overlaps that of the other semiconductor [Fig. 1(c)]. Type-II heterojunctions can be exploited to fabricate photodetectors and photovoltaic devices based on PN junctions [14–41]. In type-III heterojunctions, the semiconductor bandgaps do not overlap [Fig. 1(d)]. By forming type-III heterojunction structures, highly doped PN junctions can be obtained without the use of electrostatic or chemical doping techniques, thus facilitating easy fabrication of tunneling devices such as negative differential resistance (NDR) devices [25,26]. Moreover, vertical vdW heterostructures offer numerous possibilities for realizing high-performance electronic and optoelectronic devices. Monolayer graphene can be used as electrodes with tunable work-function because the Fermi level of graphene can be modulated by an external field due to its low density of states. Thus, a graphene electrode enables realization of vertical field effect transistors (V-FET) with a very low operating bias (below 0.5 V), high on/off-current ratio (above 10^4), and high on-current density (~1000 A/cm^2), where the graphene source electrode is vertically stacked with other vdW channel materials [42–52]. Moreover, collection of photo-generated carriers can be improved in photodetectors and photovoltaic devices by using vertically stacked heterojunction structures because of the parallel geometry of the external electric field with respect to the current direction [28–36,38–41]. In 2010, Dean et al. [53] first demonstrated a vdW heterostructure by stacking graphene onto *h*-BN, where *h*-BN was used to reduce phonon scattering for enhanced the charge transport of graphene transistors. Since then, vdW heterostructures have received significant attention in the past few years with extensive experiments focused on improving the electrical and optoelectrical performance.

In this review paper, we first introduce commonly used transfer and synthesis techniques to form vdW heterojunction structures (Section 2). We then discuss recent progress in vdW heterostructure-based electronic and optoelectronic devices, including V-FETs, NDR devices, memories, photodetectors, photovoltaic devices, and LEDs (Section 3). Finally, perspectives on future vdW heterostructure-based applications are discussed (Section 4).

2. Implementation of van der Waals heterojunctions

The development of advanced devices based on various vdW heterojunction structures provides tremendous opportunities to extend the versatility of vdW materials. Methods to form vdW heterojunction structure include mechanical transfer (top-down) and direct growth (bottom-up) processes. Usually, direct growths of vdW heterostructure allows a more controlled environment and a scalable process. Shi et al. synthesized a MoS_2/graphene heterostructure on Cu foil [54]. The precursor, ammonium thiomolybdate, together with an organic solvent was flown to the graphene surface by Ar carrier gas. The precursor self-assembled to form MoS_2 on the graphene surface via thermal decomposition with increasing temperature. Gong et al. reported a one-step growth strategy for implementing a WS_2/MoS_2 heterostructure by controlling the growth temperature [55]. MoS_2 grew first due to its high nucleation and growth rate during vapor phase reaction. The difference of their nucleation and growth rates led to sequential growth of MoS_2 and WS_2 [Fig. 2(a)]. However, this one-step growth technique has limitations in terms of the area of the grown heterostructures. Thus, Gong et al. demonstrated a two-step CVD method for growing $MoSe_2/WSe_2$ heterostructure [56]. This two-step growth method allowed spatial and size control of each vdW material [Fig. 2(b)]. But its developments are largely constrained by high wetting barrier at the vdW surface, and growth compatibility for different vdW materials [57]. Thus, the material quality and availability are limited for directly grown vdW heterostructure. So far, the majority of works in the synthesis of vdW heterostructure are achieved by mechanical transfer. A clean and repeatable transfer method for stacking vdW materials through top-down approach is of great interest. Dean et al. [53] first developed a mechanical transfer technique using polymer supporting films [Fig. 3(a)] to successfully stack monolayer graphene onto *h*-BN. This transfer process was carried out as follows: *i*) Graphene was exfoliated onto polymer films consisting of a water-soluble layer (polyvinyl alcohol; PVA) and a handling layer [poly(methyl methacrylate); PMMA]. *ii*) The stack was immersed in a deionized water bath to dissolve the water-soluble polymer layer, leaving the graphene/PMMA layer to

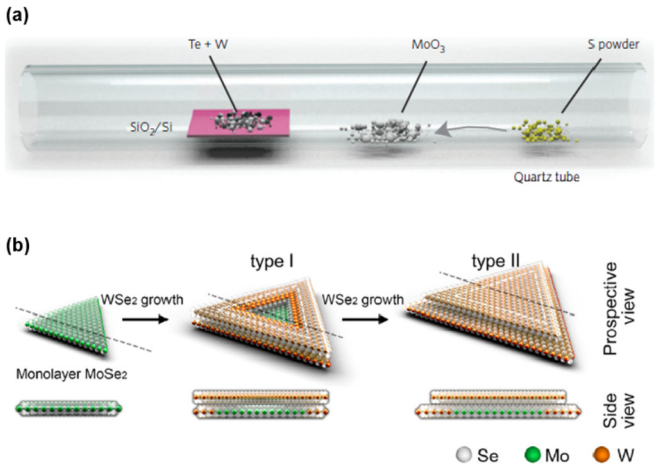

Fig. 2. (a) Schematic of the synthesis process for vdW heterostructure (reproduced with permission from Ref. [55] Copyright 2014, Nature Publishing Group). (b) Schematics of the $MoSe_2$-templated WSe_2 growth (reproduced with permission from Ref. [56] Copyright 2015, American Chemical Society). (A colour version of this figure can be viewed online.)

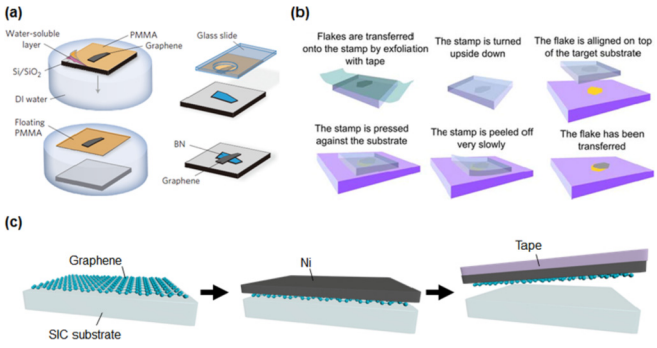

Fig. 3. (a) Schematic diagram of the PMMA-based transfer process to form graphene/*h*-BN heterostructure (reproduced with permission from Ref. [53] Copyright 2010, Nature Publishing Group). (b) Schematic illustration of the PDMS-based transfer process showing the transfer of a vdW material (donor material) onto the top of another vdW material (acceptor material) (reproduced with permission from Ref. [58] Copyright 2014, IOP Publishing Ltd). (c) Schematic diagram of the method for transferring large-scale graphene from a SiC surface onto another substrate (SiO_2/Si substrate) using stressed Ni film. (A colour version of this figure can be viewed online.)

float on the water surface. *iii*) The floating graphene/PMMA layer was transferred onto a glass slide. iv) Through the use of a micromanipulator mounted on an optical microscope, the graphene layer was precisely transferred onto a *h*-BN flake (the target vdW material) that was exfoliated onto a SiO_2/Si substrate. The target substrate was then heated to 110 °C to improve the adhesion. *v*) After transfer, the PMMA layer was removed in acetone. In 2014, Castellanos-Gomez et al. [58] presented an all-dry transfer method without involvement of wet chemistry [Fig. 3(b)]. Similar to the above mechanical transfer methods [53,58–60], a vdW material (donor material) was exfoliated onto a polydimethylsiloxane (PDMS)-based gel using tape (blue Nitto tape). Then, using a micromanipulator, the donor vdW material was transferred onto another vdW material (acceptor material) from the PDMS using a slow peel-off process. This is possible due to the viscoelastic property of PDMS allowing the donor vdW material to preferentially adhere to the acceptor vdW material and peel-off from PDMS. Recently, Kim et al. [61] proposed metal-induced transfer method at the wafer-scale, in which graphene grown on SiC was exfoliated *via* deposition of a stressed Ni film followed by an immediate transfer onto a host substrate via dry bonding process, ensuring ultra-cleanliness of the graphene/substrate interface [Fig. 3(c)]. The detailed process was carried out as follows: *i*) Ni film was deposited onto graphene grown on a SiC substrate *via* thermal evaporation. *ii*) This graphene was exfoliated from the substrate *via* the Ni layer and thermal release tape (handling layer). Here, the exfoliation of graphene was induced by the accumulated internal strain of the Ni and the relatively strong adhesion between Ni and graphene. *iii*) After exfoliation, the layer consisting of thermal release tape, Ni, and graphene was transferred onto a target substrate. *iv*) Finally, the thermal release tape was removed by annealing at 90 °C, then the Ni layer was etched by $FeCl_3$ solution. These transfer techniques have been commonly used to implement diverse electronic and optoelectronic devices based on vdW heterojunction structure, which will be introduced in the following section.

3. Van der Waals heterojunction-based electronic & optoelectronic devices

Vertically stacked heterostructures based on vdW materials (*e.g.,* graphene, transition metal dechalcogenides (TMDs), *h*-BN, and BP) have been recently used for implementing advanced electronic and optoelectronic devices. Since vdW materials do not present dangling bonds on their surfaces, one can easily form various types of heterojunctions (type-I, -II, and -III) with high-quality interfaces. The formation of such heterojunction structures offers many possibilities to design novel electronic devices with unique functionalities, such as V-FETs, NDR devices, and non-volatile memories that can be difficult to implement with a single vdW material. A tunable Schottky barrier can be easily formed by vertically stacking vdW semiconducting materials onto graphene, which enables the implementation of V-FET structures. A *h*-BN, a wide bandgap (approximately 6 eV) vdW material, provides a tunneling barrier with a high-quality interface for non-volatile memory applications. In addition, vdW heterojunctions based on type-II band alignment show extremely fast charge transfer (*e.g.,* 50 fs for hole transportation from MoS_2 to WS_2) [62,63], allowing for their implementation in ultrafast photodetection. Vertical vdW heterojunction photodetectors also exhibit high quantum efficiencies due to their fully depleted channels, which lead to minimal recombination loss of photocarriers [*e.g.,* peak external quantum efficiency (EQE) of 55% in a graphene/MoS_2/graphene heterojunction photodetector] [29]. In this section, we briefly review recent progress in vdW heterostructure-based electronic and optoelectronic devices such as V-FETs, NDR devices, memories, photodetectors, solar cells, and LEDs (Tables 1 and 2).

3.1. VdW heterojunction electronic devices

3.1.1. Vertical field effect transistors (V-FETs)

V-FETs consisting of graphene and other vdW materials have received considerable attention because they operate at voltages below 0.5 V, which is difficult to achieve in lateral FETs due to challenges in fabricating short channel devices. In V-FETs, the source-to-drain current flows vertically through the vdW materials, thus the channel length is equal to the thickness of the channel material. In addition, V-FET devices have a distinctive operating mechanism: the current is modulated by controlling the Fermi level of the graphene as source electrode, which changes the injection barrier height between the source electrode and the vdW channel [42–52]. The operations of V-FETs can be categorized as thermionic emission, direct tunneling, and trap-assisted tunneling [Fig. 4(a)]. If the barrier height between graphene and the vdW channel material is less than 0.4 eV, the V-FET mainly operates under the thermionic emission mechanism. However, if the barrier height is

Table 1
Electronic applications based on vdW heterojunction structures.

V-FET[a]	Structure	Operating mechanism	Device performance On/off-current ratio (A/A)	Operating voltage (V)	Ref.
	Gr[b]/MoS_2	Thermionic emission	1.5×10^4	0.1	[42]
	Gr/MoS_2		2.0×10^5	0.1	[43]
	Gr/MoS_2		1.0×10^5	0.5	[44]
	Gr/MoS_2		5.0×10^4	0.1	[45]
	Gr/MoS_2		1.0×10^4	0.5	[46]
	Gr/MoS_2		1.0×10^5	1	[47]
	Gr/WS_2/Gr		1.0×10^6	0.2	[48]
	Gr/$MoSe_2$		1.0×10^5	0.1	[49]
	Gr/BP[c]		8.0×10^2	0.2	[50]
	Gr/*h*-BN[d]/Gr	Direct tunneling	5.0×10^1	0.2	[51]
	Gr/WSe_2	Trap-assisted tunneling	5.0×10^7	0.1	[52]

NDR[e] device	Structure	Operating mechanism	Device performance PVCR (A/A)	Ref.
	Mono-Gr[f]/*h*-BN/Mono-Gr	Resonant tunneling	4 (at 7 K)	[14]
	Mono-Gr/*h*-BN/Mono-Gr		2 (at 2 K)	[15]
	Mono-Gr/*h*-BN/Mono-Gr		3.5 (at 300 K)	[16]
	Bi-Gr[g]/*h*-BN/Bi-Gr		1.43 (at 10 K)	[17]
	Bi-Gr/*h*-BN/Bi-Gr		1.64 (at 300 K)	[18]
	ML-Gr[h]/*h*-BN/ML-Gr		1.2 (at 300 K)	[19]
	Bi-Gr/WSe_2/Bi-Gr		6 (at 1.5 K)	[20]
	MoS_2/WSe_2/Gr		2.3 (at 300 K)	[21]
	WSe_2/$MoSe_2$/Gr		2.2 (at 300 K)	[21]
	NbS_2/MoS_2/NbS_2		4 (at 300 K)	[22]
	MoS_2/WSe_2	Band-to-band tunneling	1.86 (at 77 K)	[23]
	MoS_2/WSe_2		1.6 (at 300 K)	[24]
	BP/$SnSe_2$		1.8 (at 300 K)	[25]
	BP/ReS_2		6.9 (at 180 K)	[26]

Memory	Structure	Drain voltage (V)	Device performance P/E current ratio (A/A)	Retention time (s)	Ref.
	Gr/*h*-BN/MoS_2	0.05	1.0×10^6	1.4×10^3	[76]
	Gr/*h*-BN/MoS_2	0.05	1.0×10^6	1.0×10^5	[79]
	Gr/*h*-BN/$MoSe_2$	0.05	1.0×10^5	4.0×10^2	[77]
	Gr/*h*-BN/WS_2	0.1	4.0×10^3	2.0×10^4	[78]

[a] V-FET, Vertical field-effect transistor.
[b] Gr, Graphene.
[c] BP, Black Phosphorus.
[d] *h*-BN, Hexagonal boron nitride.
[e] NDR, Negative differential resistance.
[f] Mono-Gr, Monolayer graphene.
[g] Bi-Gr, Bilayer graphene.
[h] ML-Gr, Multilayer graphene.

larger than 0.4 eV, the thermionic emission process is suppressed and direct tunneling dominates the current of the V-FETs, given the condition that the vdW materials is thin enough to induce direct tunneling (below 5 nm). Lastly, if the vdW materials have high trap densities, the V-FET is likely to operate under the trap-assisted tunneling mechanism [52].

Yu et al. [42] and Georgiou et al. [48] demonstrated V-FETs based on graphene/MoS_2 and graphene/WS_2 heterojunction structures, respectively. In the MoS_2- and WS_2-based V-FET devices, the carrier transport mechanism was mainly based on the thermionic emission phenomenon, because low injection barrier height is formed between the graphene and the vdW materials (0.15 eV for graphene/MoS_2 and 0.3 eV for graphene/WS_2). Under a positive gate voltage, electron carriers easily overcome the barrier between the graphene and the vdW materials as the Fermi level of graphene is up-shifted and the barrier height is reduced. In contrast, under a negative gate voltage, the barrier height increases because of the down-shift in the Fermi level of graphene, which suppresses the transport of electrons from the graphene (source) to the vdW materials (channel). Based on this operation mechanism, these V-FET devices exhibited high on/off current ratios at a very low operating voltage of 0.1 V, which were approximately 10^3 and 10^6 for the graphene/MoS_2 and graphene/WS_2 V-FETs, respectively [Fig. 4(b)]. Similarly, Kang et al. [50] reported a V-FET device based on graphene/BP heterojunctions that also operates based on thermionic emission mechanism. However, this device demonstrated relatively low on/off current ratio of 42 at room temperature, since a low barrier height (<0.01 eV) forms between graphene and BP. Another type of V-FET device based on a graphene/*h*-BN/graphene heterojunction structure was reported by Britnell et al. [51] The V-FET device operated by direct tunneling, due to a large barrier height for holes between graphene and *h*-BN (1.5 eV). The significantly larger barrier height at the graphene/*h*-BN junction poses challenges for barrier modulation by gate biasing, resulting in an inefficient current control [Fig. 4(c)]. Therefore, this device exhibited a much lower on/off current ratio (approximately 50) as compared to previous graphene/TMD V-FET devices that operated by the thermionic emission [Fig. 4(d)]. Recently, Shim et al. [52] observed that the trap-assisted tunneling mechanism dominating the source-to-drain current of a graphene/WSe_2 V-FET device. This new mechanism is enabled by a moderate barrier height of 0.51 eV forming at the graphene/WSe_2 junction and a large trap density in WSe_2 near the Dirac point of the graphene, as high as 1.05×10^{12} cm^{-2}. Here, the probability of empty states at the energy level of the WSe_2 traps was exponentially decreased as the gate voltage increased. This V-FET device exhibited a high on/off

Table 2
Optoelectronic applications based on vdW heterojunction structures.

Photodetector	Structure	Incident laser Wavelength (nm)	Power (μW)	Device performance Responsivity (A/W)	Switching speed (s)	Ref.
	Gr[a]/WS_2/Gr	633	10	1.0×10^{-1}	–	[28]
	Gr/MoS_2/Gr	488	10	2.2×10^{-1}	–	[29]
	Gr/$MoTe_2$/Gr	1064	2	1.1×10^{-1}	2.4×10^{-5}	[30]
	WSe_2/Gr/MoS_2	532	0.001	2.0×10^{3}	3.0×10^{-5}	[31]
	h-BN[b]/Gr/WSe_2/Gr/*h*-BN	759	5	1.8×10^{-2}	5.5×10^{-12}	[32]
	h-BN/Gr/BP/Gr/*h*-BN	1550	–	–	1.0×10^{-10}	[33]

Photovoltaic device	Structure	Incident light source	Device performance PCE[c] (%)	EQE[d] (%)	Ref.
	WSe_2/MoS_2	Halogen lamp	0.2	1.5	[34]
	WSe_2/MoS_2	AM 1.5G	0.15	0.1	[35]
	WSe_2/MoS_2	514 nm	–	12	[36]
	WSe_2/MoS_2	AM1.5G	0.4	>50	[37]
	Gr/WSe_2/MoS_2/Gr	532 nm	–	34	[38]
	GaTe/MoS_2	473 nm	0.45	61.68	[39]
	GaTe/MoS_2	514 nm	–	266	[40]
	$ReSe_2$/MoS_2	633 nm	–	1266	[41]

LED[e]	Structure	SQW[f]/MQW[g]	Device performance EL[h] peak position (nm)	EL efficiency (%)	Ref.
	Gr/*h*-BN/$MoSe_2$/*h*-BN/Gr	SQW	770	5	[8]
	Gr/*h*-BN/WSe_2/*h*-BN/Gr		760	1	[8]
	Gr/*h*-BN/WSe_2/*h*-BN/Gr		751	–	[9]
	Gr/*h*-BN/WSe_2/*h*-BN/Gr		740	0.2	[10]
	Gr/*h*-BN/WSe_2/*h*-BN/Gr		748	–	[11]
	Gr/*h*-BN/WSe_2/*h*-BN/Gr		740	–	[12]
	Gr/*h*-BN/WS_2/*h*-BN/Gr		606	1	[13]
	Gr/h-BN/WSe2/h-BN/Gr	MQW	660	8.4	[13]

[a] Gr, Graphene.
[b] *h*-BN, Hexagonal boron nitride.
[c] PCE, Power conversion efficiency.
[d] EQE, External quantum efficiency.
[e] LED, Light-emitting diode.
[f] SQW, Single-quantum well.
[g] MQW, Multi-quantum well.
[h] EL, Electroluminescence.

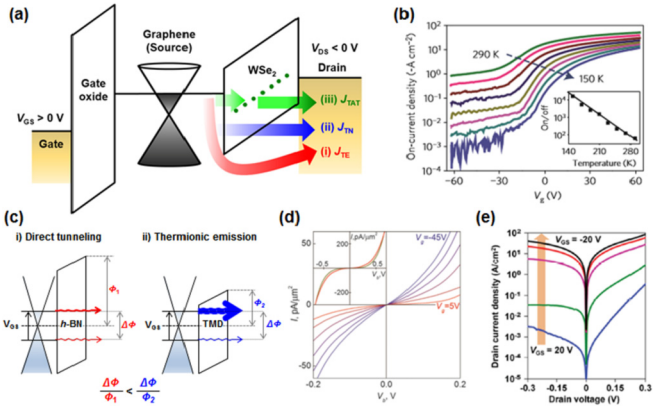

Fig. 4. (a) Energy band diagram of a V-FET device under positive gate and negative drain biases. Red, blue, and green arrows indicate (*i*) thermionic emission, (*ii*) direct tunneling, and (*iii*) trap-assisted tunneling currents (reproduced with permission from Ref. [52] Copyright 2016, WILEY-VCH). (b) Electrical characteristics (J_D–V_G) of a graphene/MoS_2 heterojunction-based V-FET at different measurement temperatures between 290 and 150 K. The inset shows the extracted on/off-current ratios as a function of measurement temperature (reproduced with permission from Ref. [42] Copyright 2013, Nature Publishing Group). (c) Energy band diagrams of graphene/*h*-BN (operated with direct tunneling mechanism) and graphene/TMD heterojunction-based V-FETs (operated with thermionic emission mechanism). (d) J_D–V_D curves of a graphene/*h*-BN heterojunction-based V-FET with varying gate biases between 5 V and −45 V (reproduced with permission from Ref. [51] Copyright 2012, American Association for the Advancement of Science). (e) Electrical characteristics (J_D–V_D) of a graphene/WSe_2 heterojunction-based V-FET under various gate biases between −20 and 20 V (reproduced with permission from Ref. [52] Copyright 2016, WILEY-VCH). (A colour version of this figure can be viewed online.)

current ratio of approximately 3×10^4 at room temperature (5×10^7 at 180 K) [Fig. 4(e)]. The V-FETs mentioned above are promising candidates for next-generation low-power electronic devices in industrial scale.

3.1.2. Negative differential resistance devices

NDR devices have been considered as one of the most promising candidates for realizing multi-valued logic (MVL) circuits, that can process information with reduced memory elements and interconnections, as compared to traditional binary logic circuits [24,26,27,64–67]. In an NDR devices, multiple threshold voltages exist in a bias region, where the driving current has a negative dependence on voltage bias. By leveraging these multiple operating regions, in which the driving current increases toward each peak point, a multi-valued inverter for MVL can be implemented by using a p-channel transistor as a load resistor [24,26,27]. This NDR characteristic can be achieved by using the tunneling mechanism in various types of semiconductor heterojunction structures [14–27,68–75]. However, it is currently difficult to form high-quality heterojunctions with conventional semiconductors (*e.g.*, Si, Ge, and III-V compound semiconductors), because of crystallographic defects caused by lattice mismatch at the junction interfaces. Although super-lattice and nanowire structures have been proposed to overcome this lattice mismatch, the actual implementation is challenging due to the process complexity [68–75]. Very recently, vdW material-based heterojunctions have become attractive alternatives for next-generation NDR devices as vdW materials offer defect-free interface for various heterostructures

[2–5]. In this section, we review the vdW heterojunction-based resonant tunneling diodes (RTDs) and Esaki diodes, which are the representative devices showing NDR characteristics.

Britnell et al. [14] demonstrated a RTD device based on a graphene/*h*-BN/graphene heterojunction, in which resonant tunneling occurs when the Fermi level of the bottom graphene electrode aligns to that of the top graphene electrode [Fig. 5(a)]. The peak-to-valley current ratio (PVCR) of the RTD device varied from 1.5 to 4.0 with increasing gate voltage from −55 to 15 V, as shown in Fig. 5(b). As the gate voltage is changed, the Fermi level of graphene is adjusted in accordance, resulting in a PVCR value that depends on the gate voltage. Kang et al. [18] also reported a gate-tunable RTD device based on a heterojunction structure consisting of *h*-BN sandwiched between two bilayer graphene electrodes. Bilayer graphene present two sub-bands (lower and upper bands) which allow resonant tunneling to occur more than once when *i*) the charge neutrality regions of the top and bottom layers are aligned [case I in Fig. 5(c)], and *ii*) the upper (or lower) band of one layer is aligned with that of the other layer [case II in Fig. 5(c)]. Consequently, this gate-tunable RTD device exhibits multiple NDR peaks with PVCR values of 1.2–1.5 [Fig. 5(d)]. This NDR characteristic can be also obtained through the implementation of an Esaki diode. Roy et al. [23] demonstrated an Esaki diode using a MoS_2/WSe_2 heterojunction structure, where a dual-gate structure is used to independently modulate the electrostatic potentials of the MoS_2 and WSe_2 layers, achieving a p^+/n^+ junction as shown in Fig. 6(a). When a low drain voltage is applied [bias I in Fig. 6(b)], the electrons tunnel from the conduction band of MoS_2 to the valence band of WSe_2 (band-to-band tunneling). This tunneling current increases until the conduction band edge of MoS_2 is aligned with the valence band edge of WSe_2. When the applied drain voltage further increases [bias II in Fig. 6(b)], the band-to-band tunneling is suppressed because the Fermi levels of both MoS_2 and WSe_2 enter the forbidden band regions of counterpart materials, inducing the NDR characteristic with a high PVCR of 3 [Fig. 6(c)]. In addition, an NDR device with a very high PVCR of 4.2 at room temperature was recently realized by Shim et al., without forming heavily doped regions in a BP/rhenium disulfide (ReS_2) heterojunction structure [Fig. 6(d)] [26]. This NDR device was achieved through broken-gap band alignment that could induce a heavily doped n^+/p^+ junction at the junction interface without the use of chemical or electrostatic doping processes. In this report, a ternary inverter with three logic states was demonstrated by integrating a BP/ReS_2 heterojunction-based NDR device with a BP p-channel transistor. Very recently, Shim et al. also reported a light-induced negative differential transconductance (L-NDT) phenomenon in a three-terminal MVL device based on a graphene/WSe_2 heterojunction structure [Fig. 6(e)] [27]. In general, the drain photocurrent in n-channel transistors increases continuously with increasing gate voltage in the positive direction (or negative direction for p-channel devices) under light illumination. In contrast, the graphene/WSe_2 heterojunction-based device demonstrated a reduction in drain photocurrent with increasing gate voltage, exhibiting an abnormal I_D–V_G characteristic curve with two threshold voltages, which is an indication of L-NDT phenomena. By using the graphene/WSe_2 heterojunction-based L-NDT device, the authors implemented a ternary inverter circuit having three stable logic states [Fig. 6(f)]. These studies on NDR and L-NDT devices based on vdW heterojunction structures are expected to open up new opportunities for future low power electronics technology.

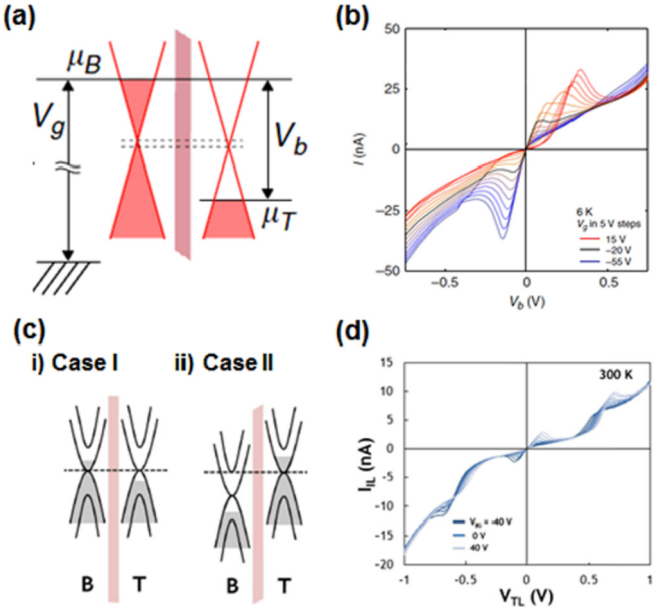

Fig. 5. (a) Energy band diagram of a graphene/*h*-BN/graphene heterojunction-based RTD under gate bias of 15 V. (b) Measured *I*-*V* characteristics of the graphene/*h*-BN/graphene heterojunction RTD at 6 K (reproduced with permission from Ref. [14] Copyright 2013, Nature Publishing Group). (c) Band diagrams of a bilayer graphene/*h*-BN/bilayer graphene heterojunction RTD with different band alignment conditions. (d) *I*-*V* curves of the bilayer graphene/*h*-BN/bilayer graphene heterojunction RTD showing multiple NDR peaks (reproduced with permission from Ref. [18] Copyright 2015, Institute of Electrical and Electronics Engineers). (A colour version of this figure can be viewed online.)

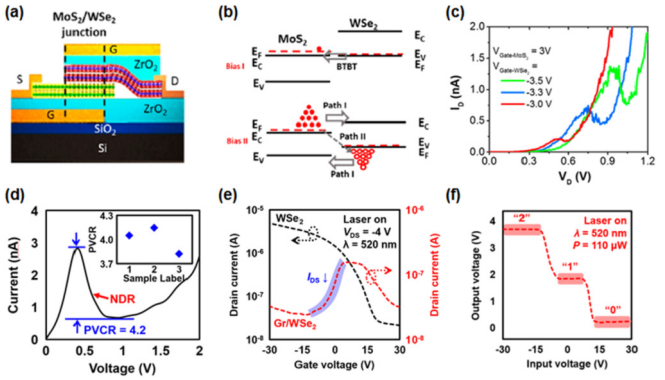

Fig. 6. (a) Schematic of a MoS_2/WSe_2 heterojunction-based Esaki diode. (b) Band diagrams corresponding to the peak- and valley-current conditions under different biases in the MoS_2/WSe_2 heterojunction-based Esaki diode. (c) *I*-*V* characteristics of the MoS_2/WSe_2 heterojunction-based Esaki diode with varying WSe_2-side gate bias (reproduced with permission from Ref. [23] Copyright 2015, American Chemical Society). (d) I_D–V_D curve of a BP/ReS_2 heterojunction-based NDR device. The inset shows the extracted PVCR values of the three different NDR devices (reproduced with permission from Ref. [26] Copyright 2017, Nature Publishing Group). (e) I_D–V_G curves of a conventional WSe_2 transistor and a graphene/WSe_2 heterojunction-based L-NDT device under light illumination conditions. (f) Voltage transfer characteristic of a ternary inverter formed with the graphene/WSe_2 heterojunction-based NDT device and p-channel WSe_2 TFT (reproduced with permission from Ref. [27] Copyright 2017, American Chemical Society). (A colour version of this figure can be viewed online.)

3.1.3. Non-volatile memory devices

Recently, vdW materials have also been investigated for floating gate-based memory devices that operate by detecting the presence of trapped charges in the floating gate region. Floating gate devices formed with vdW materials respond to minute changes in external electric field due to its atomic-scale thicknesses, allowing high programming/erasing (P/E) current ratios. Furthermore, by forming an ideal potential well with high quality heterogeneous interface, a large amount of charges can be stored in the floating gate of vdW memory devices, resulting in an increased retention time. This is

enabled by the stacking of defect-free vdW materials with various bandgaps. In this section, we introduce high-performance floating gate memory devices consisting of vdW materials.

Choi et al. [76] fabricated a floating gate memory device by using a graphene/*h*-BN/MoS_2 heterostructure, where monolayer MoS_2, graphene, and *h*-BN were used as the channel, floating gate, and tunneling barrier layers, respectively [Fig. 7(a)]. The excellent gate controllability of the MoS_2-channel transistor enables memory devices to achieve a high P/E current ratio of approximately 10^3. In particular, the high P/E current ratio was maintained for more than 1400 s with minimal degradation of P/E current ratio (less than 10%) [Fig. 7(b)]. Similar floating gate memory devices with $MoSe_2$ and WS_2 channel materials were reported by Cheng et al. [77] and Qiu et al. [78], respectively. These memory devices also produced high P/E current ratios of 10^3 and reliable data retention for more than 10 years, as shown in Figs. 7(c) and (d). Meanwhile, Vu et al. [79] demonstrated a two-terminal floating gate memory device with a significantly higher P/E current ratio of 10^9 and a data retention time of 10^4 s. This device was fabricated by stacking monolayer MoS_2, *h*-BN, and monolayer graphene. When a negative drain bias (−6 V) is applied, a large potential difference between the floating gate (graphene) and the drain electrode induces electron tunneling into the floating gate through the *h*-BN dielectric layer (programming process). Although the trapped electrons cause a potential difference between the source electrode and the graphene floating gate (−2.27 V), this is sufficiently low such that no trapped electrons are lost [Fig. 7(e)]. Conversely, when a positive drain bias (+6 V) is applied, holes tunnel from the drain electrode to the graphene (erasing process). The high performance demonstrated by vdW material-based memory devices, as shown through high P/E current ratios (above 10^3) and stable retentions (above 10^3 s), offer a promising route towards future memory devices.

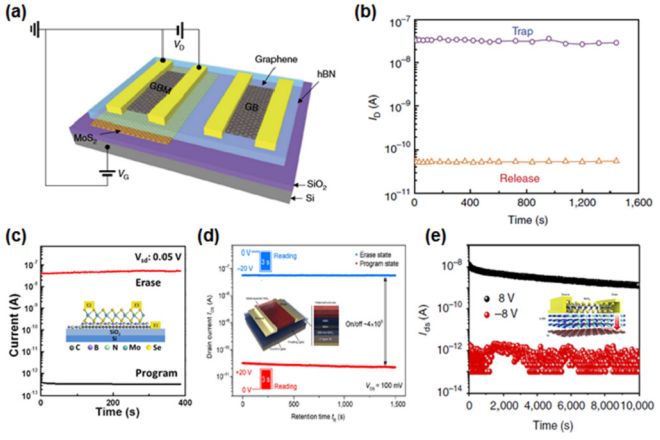

Fig. 7. (a) Schematic of a graphene/*h*-BN/MoS_2 heterojunction-based memory device. (b) Retention characteristics of the graphene/*h*-BN/MoS_2 heterojunction memory device. For the retention measurement, pulses of −15 V (programming process) and +15 V (erasing process) were used (pulse width = 100 μs) (reproduced with permission from Ref. [76] Copyright 2013, Nature Publishing Group). (c) Retention characteristics of the graphene/*h*-BN/$MoSe_2$ heterojunction memory device at −80 V (programming process) and +80 V (erasing process) (reproduced with permission from Ref. [77] Copyright 2017, AIP Publishing). (d) Retention characteristics of the graphene/*h*-BN/WS_2 heterojunction memory device after applying voltage pulses (±20 V and $\Delta t = 3$ s) (reproduced with permission from Ref. [78] Copyright 2016, Springer International Publishing AG). (e) Retention characteristics of the graphene/*h*-BN/MoS_2 heterojunction memory device. Program and erase states were obtained by applying voltage pulses (±8 V with pulse width of 0.1 s) (reproduced with permission from Ref. [79] Copyright 2016, Nature Publishing Group). (A colour version of this figure can be viewed online.)

3.2. VdW heterojunction optoelectronic devices

3.2.1. Photodetectors

A photodetector is an optoelectronic device that converts light into electrical signals by absorbing light with the photon energy larger than the band gap energy of the semiconductor, generating electron–hole pairs. Recently, vdW materials were utilized to implement photodetectors with high photoresponsivity and detection speed. For example, TMD materials exhibited strong light-matter interaction and high light absorbance, allowing high photoresponsivity up to 10^7 A/W [80–102]. Moreover, graphene's extremely high mobility of approximately 200,000 $cm^2 V^{-1} s^{-1}$ [103] enables the realization of an ultrafast photodetector with an optical data transfer rate of 10 Gbit s^{-1}. Lately, to further improve the photoresponsivity and switching speed, heterostructures consisting of various vdW materials have been applied to the fabrication of photodetectors [28–33]. In this section, we introduce vdW heterostructure-based photodetectors with high photoresponsivity and fast switching speed.

Britnell et al. [28] demonstrated a high-performance photodetector based on a graphene/WS_2/graphene heterostructure, where a 5-nm-thick WS_2 and monolayer graphene was used as the light-absorbing layer and the transparent electrode, respectively [Fig. 8(a)]. The Fermi level of graphene is modulated through electrostatic gating, and the direction of the external field is parallel to that of the current flow in this heterojunction device. Consequently, the separation and transportation of the generated electron–hole pairs can be directly controlled by an external gate field without recombination loss of photocarriers [Fig. 8(b)]. Such photodetectors exhibited a relatively high photoresponsivity of 0.1 A/W as compared to that of a lateral WS_2 photodetector (approximately 1 mA/W) [104], under the same excitation intensity [Fig. 8(c)]. Graphene/TMD/graphene photodetectors using MoS_2 and $MoTe_2$ as the light absorbers were reported by Yu et al. [29] and Zhang et al. [30], respectively. These photodetectors also present high photoresponsivity values of 0.22–0.2 A/W, under the

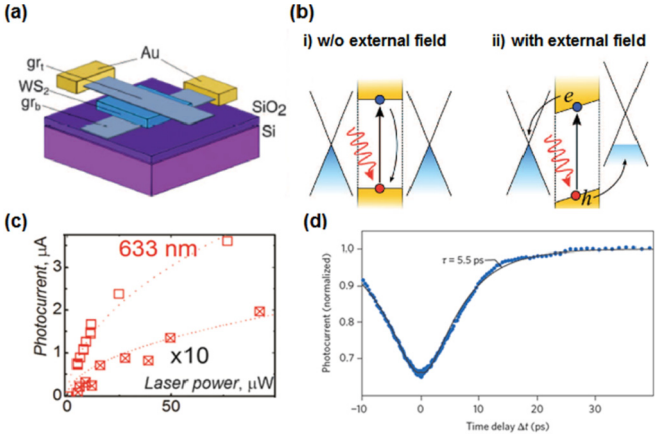

Fig. 8. (a) Schematic illustration of a graphene/WS_2/graphene heterojunction-based photodetector. (b) Energy band diagrams for the graphene/WS_2/graphene heterojunction photodetector *i*) without and *ii*) with an external field. (c) Measured photocurrent of the graphene/WS_2/graphene heterojunction photodetector as a function of laser intensity power, where the wavelength of the laser was 633 nm. Open square symbols are for a device on Si/SiO_2 substrate and square with cross symbols are for a device on a polyethylene terephthalate (PET) substrate (reproduced with permission from Ref. [28] Copyright 2012, American Association for the Advancement of Science). (d) Normalized photocurrent of a *h*-BN/graphene/WSe_2/graphene/*h*-BN heterojunction photodetector as a function of time delay between two laser pulses (reproduced with permission from Ref. [32] Copyright 2016, Nature Publishing Group). (A colour version of this figure can be viewed online.)

illumination of 480-nm laser at 5 μW. In addition, the switching speed of photodetectors can be enhanced by employing vdW heterostructures. Massicotte et al. [32] reported a high-speed photodetector based on a graphene/WSe_2/graphene heterojunction encapsulated by *h*-BN layers with a reported switching time of 5.5 ps [Fig. 8(d)], approximately 10^7-fold shorter than that of a lateral WSe_2 photodetector (<50 μs [95]). This fast switching was accomplished by *i*) the short transport distance between the top and bottom graphene electrodes and *ii*) the *h*-BN, free charge trapping, passivation to improve the charge transport in graphene. Overall, the use of vdW heterojunction structures for photodetectors provides a promising solution for realizing future photodetectors with fast photoresponse and switching speed.

3.2.2. Photovoltaic devices

PN junctions allow efficient separation of the photo-generated electron and hole carriers at the junction interface to induce the photovoltaic effect. As mentioned previously, various PN junctions can be easily implemented by stacking p- and n-type vdW materials. The vertical stacking of multiple PN junctions, corresponding to different absorption energies, can be achieved without the concerns of lattice mismatch. Thus, the vdW materials have recently been considered as promising materials for the next-generation of thin film photovoltaic cells. Bernardi et al. claimed that 2–3 times higher power conversion efficiency (PCE) can be obtained in vdW materials-based photovoltaic devices than other ultrathin photovoltaic devices [105]. In this section, we introduce highly efficient photovoltaic devices fabricated on various vdW hetero-PN-junction structures.

Furchi et al. [34] first demonstrated a vdW PV device by using a hetero-PN junction that consisted of p-type WSe_2 and n-type MoS_2. By adjusting the doping level of the vdW materials by controlling the gate voltage, the authors formed a high built-in potential in the hetero-PN-junction, consequently showing a PCE of 0.2% under a gate voltage of −50 V. The photovoltaic effect is typically influenced by the built-in potential, which is a critical factor in separating photo-generated electron–hole pairs towards opposite electrodes. Similarly, Lee et al. [38] achieved a highly efficient photovoltaic device by using a WSe_2/MoS_2 hetero-PN junction with graphene as top and bottom electrodes [Fig. 9(a)]. In this device, photovoltaic properties such as open-circuit voltage, short-circuit current, and fill factor were significantly improved by increasing the number of layers of WSe_2/MoS_2 [Fig. 9(b)]. Improving the EQE and the external radiation efficiency (ERE) through gold (Au) back reflector using same process applied in thin film III-V photovoltaic devices [105,106], Wong et al. [37] demonstrated a conversion efficiency of 0.4% under AM1.5G solar spectrum with absorbance and EQE above 90% and 50% respectively. The device structure uses the same WSe_2/MoS_2 hetero-PN junction with multi-layer graphene top contact. The highest EQE value achieved in a multilayer hetero-PN-junction device was 34%, which is much higher than that of the devices composed of monolayer (2.4%) and bilayer (12%) vdW materials [Fig. 9(c)]. Recently, a GaTe/MoS_2 hetero-PN junction was exploited to implement a high-performance photovoltaic device [39]. A thick GaTe layer (14 nm), which has a direct energy bandgap regardless of its thickness, was used as a p-type vdW material. This photovoltaic device efficiently absorbed incident light, consequently exhibiting a high PCE of 0.45% and an EQE of 61.68%. These approaches to utilize various vdW hetero-PN junctions are expected to create new pathways for implementing highly efficient photovoltaic devices.

3.2.3. Light-emitting diodes

Monolayer vdW materials have high exciton binding energies because of their strong quantum confinement property, which

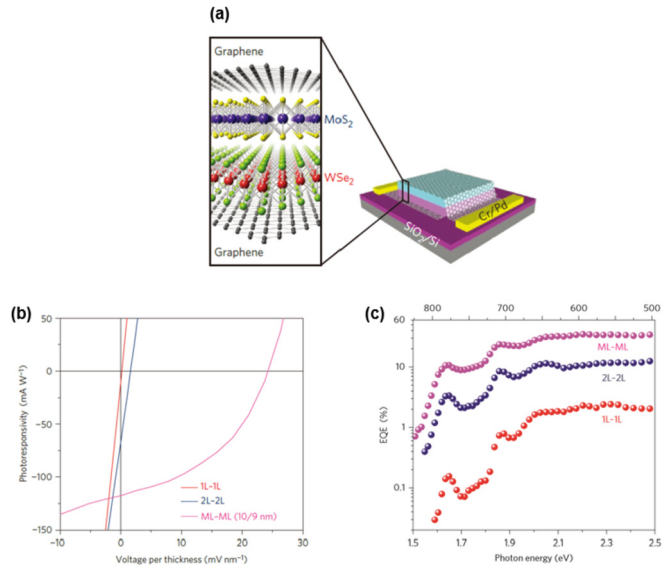

Fig. 9. (a) Schematic of a graphene/WS_2/MoS_2/graphene heterojunction-based photovoltaic device. (b) Photoresponsivity characteristics of the graphene/WS_2/MoS_2/graphene heterojunction photovoltaic devices with various layer number of WSe_2/MoS_2 heterojunction (1L–1L, 2L–2L, and ML–ML) as a function of voltage per film thickness. (c) Calculated EQE of the graphene/WS_2/MoS_2/graphene heterojunction photovoltaic devices with various vdW layer thicknesses as a function of photon energy (reproduced with permission from Ref. [38] Copyright 2014, Nature Publishing Group). (A colour version of this figure can be viewed online.)

reduces the radiative lifetime of excitons (radiative lifetime is known to be inversely proportional to the exciton binding energy) [107]. This consequently suppresses the diffusion of excitons towards the non-radiative recombination center and increases their rate of radiative recombination. Therefore, monolayer vdW materials are applicable to LED applications. Recently, several research groups have reported the fabrication of two-dimensional (2D) LEDs based on various vdW heterostructures composed of monolayer vdW materials sandwiched between *h*-BN barrier layers, to form quantum well structures [8–13]. In these works, high-quality quantum well structures without interfacial defects were achieved because of the absence of dangling bonds on the surfaces of the vdW materials. By applying this quantum well structure to LED devices, electron and hole carriers were effectively confined in the active region (quantum well), increasing the recombination rate and enhancing the luminescence efficiency of the LEDs. In this section, we briefly review 2D LEDs based on vdW quantum well structures.

Withers et al. [8] and Clark et al. [12] demonstrated 2D vdW LED devices based on a quantum well structure consisting of graphene, *h*-BN, and other vdW materials (MoS_2, $MoSe_2$, WS_2, and WSe_2), as shown in Fig. 10(a). When a positive bias is applied to the top graphene electrode, the Fermi levels of the bottom and top graphene layers respectively up-shifts over the conduction band edge and down-shifts under the valence band edge of the vdW materials that serve as the active light-emitting layer [Fig. 10(b)]. This Fermi level behavior efficiently injects many electrons and holes into the vdW emitting layer, leading to light emission via radiative recombination. In particular, the thickness of the *h*-BN layer acting as a tunneling barrier significantly affects the current-to-light conversion efficiency of these 2D LEDs. For *h*-BN with two layers or less, carriers directly tunnel from one graphene electrode to the other without accumulating in the quantum well region, consequently reducing the current-to-light conversion efficiency. However, for *h*-BN containing more than four layers, the tunneling phenomenon is

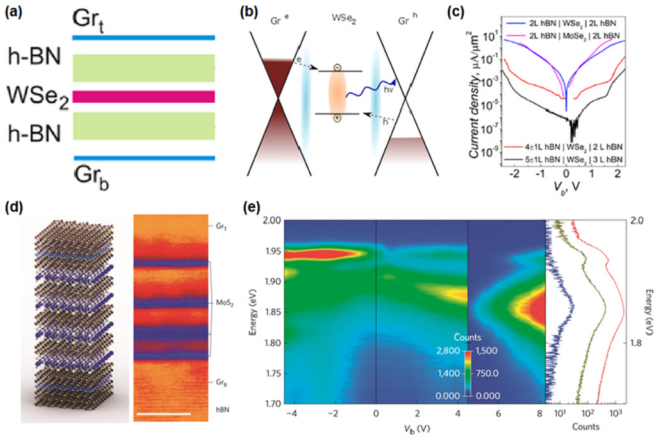

Fig. 10. (a) Schematic illustration of a graphene/*h*-BN/WSe_2/*h*-BN/graphene heterostructure (reproduced with permission from Ref. [8] Copyright 2015, American Chemical Society). (b) Energy band diagram of a graphene/*h*-BN/WSe_2/*h*-BN/graphene heterojunction-based LED. Due to the applied bias, carriers can tunnel from the graphene electrode to the WSe_2 active layer through the *h*-BN (reproduced with permission from Ref. [12] Copyright 2016, American Chemical Society). (c) Electrical characteristics of graphene/*h*-BN/WSe_2/*h*-BN/graphene and graphene/*h*-BN/$MoSe_2$/*h*-BN/graphene heterostructure-based LEDs with different *h*-BN thicknesses (reproduced with permission from Ref. [8] Copyright 2015, American Chemical Society). (d) Three-dimensional schematic and scanning transmission electron microscopy (STEM) image of multiple quantum well structure based on a *h*-BN/graphene/*h*-BN/MoS_2/*h*-BN/MoS_2/*h*-BN/MoS_2/*h*-BN/MoS_2/*h*-BN/graphene/*h*-BN heterostructure. (e) Mapping images of PL and EL spectra and individual EL spectra for a multiple quantum well LED device (reproduced with permission from Ref. [13] Copyright 2015, American Chemical Society). (A colour version of this figure can be viewed online.)

suppressed and the current drops, along with the conversion efficiency [Fig. 10(c)]. As a result, the highest electroluminescence (EL) efficiency (5%) was achieved in a 2D LED device fabricated with a quantum well structure using 2–3 *h*-BN barrier layers. To enhance the EL efficiency further, Withers et al. suggested using a multiple quantum well structure in which *h*-BN, graphene, *h*-BN, MoS_2, *h*-BN, MoS_2, *h*-BN, MoS_2, *h*-BN, graphene, and *h*-BN layers were sequentially stacked [Fig. 10(d)] [13]. In such a 2D LED device fabricated with three quantum wells, a very high EL efficiency of 8.4% was exhibited [Fig. 10(e)]. This high EL efficiency is comparable to that of modern organic LEDs [108]. These results indicate that vdW-material-based quantum well structures may serve as a promising platform for the implementation of next-generation LEDs.

4. Prospects

We conclude this review by discussing several outstanding issues related to vdW heterojunction structure-based applications and our personal perspective for future research. So far, most electronic and optoelectronic devices based on vdW heterojunction structures are still at the level of micrometer-scale fabrication technology. Furthermore, these vdW heterojunction devices are fabricated by using mechanical dry transfer processes that cause cracks, wrinkles, and other structural contaminations. Even though studies on vdW heterojunctions fabricated using chemical vapor deposition (CVD) have been recently reported, such a fabrication process is still in its infancy, showing limitations in growth area coverage, and poor electrical/optical device properties [109–115]. Thus, the device sizes were limited by transfer and growth techniques. Since high-quality vdW materials with large areas will be required for the industrialization of vdW heterojunction-based applications, the development of techniques to directly synthesize vdW materials on another vdW materials at the wafer-scale is a high priority for the successful integration of vdW heterojunction-based devices and circuits. Furthermore, a method to stack three-dimensional semiconductors has been developed recently, so called 2D material-based layer transfer (2DLT) technique. The 2DLT process will open up opportunities to stack ultrathin 3D semiconductor films together with 2D materials to form unique 3D/2D heterostructures [116]. Moreover, it would be useful to find theoretical carrier transport models that are specific to vdW heterojunction structure systems. These transport models will go beyond the existing theory of conventional three-dimensional materials and help researchers understand more deeply the operating mechanisms of their novel devices. In addition, most studies related to vdW heterostructures have focused on proof-of-concept to demonstrate the feasibility of electronic and optoelectronic devices. The researches related to *i*) integration of V-FETs and NDR/NDT devices into arithmetic circuits, *ii*) integration of photodetectors into multiple pixel arrays, and *iii*) green/blue LEDs for displays should be further investigated. Finally, we believe that the vdW heterostructures will be utilized not only for electronic and optoelectronic applications but also other functional purposes such as thermoelectronics, biosensors, energy storage, and so on due to its high electrical conductance, low thermal conductance, high surface-to-volume ratio, and short diffusion length [117,118].

Conflicts of interest

The authors declare no competing financial interest.

Acknowledgments

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